ACEEE Int. J. on Control System and Instrumentation, Vol. 4, No. 2, June 2013

Analysis and Design of CMOS Source Followers and Super Source Follower

Mr. D. K. Shedge[1], Mr. D. A. Itole[2], Mr. M. P. Gajare[3], and Dr. P. W. Wani[4]
[123] AISSMS IOIT, Electronics Engineering Dept., Pune, India
Email: dshedge@yahoo.com
[4] College of Engineering, Electronics and Telecommunication Dept., Pune, India
Email: cooldev.itole@gmail.com and pwwani@gmail.com

***Abstract*— The source follower circuit is used as a voltage buffer and level shifter. It is more flexible level shifter as the dc value of voltage level can be adjusted by changing aspect ratio of MOSFETs. It is desired to have low output resistance for such applications. Source follower can give minimum output resistance $1/(g_m+g_{mb})$ with load resistance and channel resistance tending to infinity. The super source follower is a circuit formed using negative feedback through another MOSFET. This offers even reduced output resistance but with reduced voltage gain as that of source follower.**

***Index Terms*— NMOS Source follower (NSF), PMOS Source follower (PSF), Super Source follower (SSF), Voltage buffer, Level shifter, output resistance.**

I. Introduction

A high voltage gain can be achieved from common source amplifier with high load impedance [5]. If amplifier is required to drive a low impedance load then a buffer must be placed after amplifier. A buffer will drive the low impedance load with negligible loss of signal strength [2].

The common drain stages (source followers) are used as building blocks in a large number of high speed or high frequency applications, due to their intrinsic simplicity and wideband characteristics [7] [8]. The source followers suffer from non-ideal effects such as body effect, channel length modulation, capacitive effects and distortions arising from capacitive loads. These non-ideal effects create a tradeoff among linearity, bandwidth and power dissipation. The main objective of this paper is to analyze and design the NSF, PSF and SSF for wide bandwidth with low power consumption at 2.5V supply. The analysis of source followers is based on non-linear parameters g_m, g_{mb} and r_o in a low frequency small signal model.

Section II describes the analysis of NMOS, PMOS and Super source followers with small signal low frequency models. In section III, the proposed circuits of source followers and super source follower are presented. The performances of the three source followers are observed using EDA Tool Tanner V14.1 and Cadence. Concluding remarks are made in Section IV.

II. Analysis of Source Follower

For NSF as well as PSF, the input signal is applied to the gate and output is taken from the source. For signal levels above threshold voltage, the output voltage is equal to input voltage minus gate source voltage. The gate source voltage consists of threshold and over drive voltage. If both these voltages are constant, then output voltage is simply input voltage added with offset. The small signal gain would then be unity. Thus, the source follows the gate and circuit is known as a source follower. Actually threshold voltage depends on the body effect and the over drive depends on drain current. Also even if the drain current is kept constant, the over drive depends to some extent on the drain-source voltage. Small signal equivalent circuits of MOSFETs with body effect can evaluate the analysis of source follower circuits.

B. Small Signal Analysis of NSF

The NSF in Fig. 1 consists of an NMOS input transistor and an NMOS current source as a load [9]. The input signal V_i consists of the DC biasing voltage V_{TH} and the ac signal v_i whereas the output signal V_o consists of a DC biasing voltage V_{DS} and the ac signal v_o. For n-well process, the bulks of M_1 and M_2 share the same substrate. Hence, NSF suffers from the body effect.

The small signal equivalent circuit of NSF is shown in Fig. 2. The body terminal is connected to lowest supply voltage (ground) to maintain source body junction reverse biased. Since source is connected to output, v_{bs} changes with output [1]. The load current source formed with M_2 is replaced by its drain resistance r_{o2}.

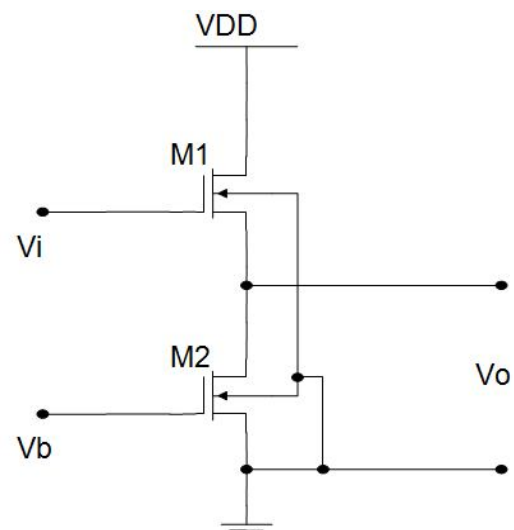

Figure 1. NMOS Source follower (NSF) circuit

DOI: 01.IJCSI.4.2.1281

ACEEE Int. J. on Control System and Instrumentation, Vol. 4, No. 2, June 2013

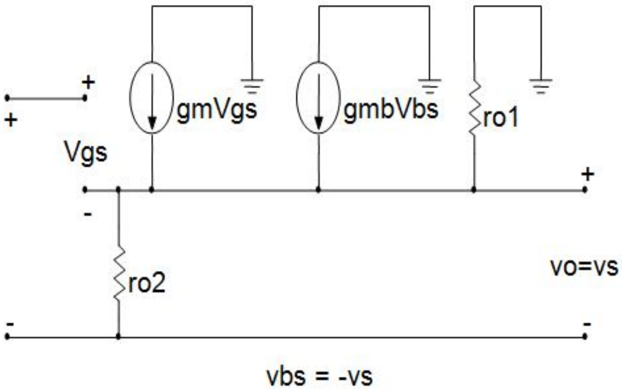

Figure 2. Small signal equivalent circuit of NSF

Applying KVL around input loop,

$$v_i = v_{gs} + v_o \tag{1}$$

When the output is open circuited, $i_o = 0$ and applying KCL at output node gives

$$g_m v_{gs} - g_{mb} v_o - \frac{v_o}{r_{o2}} - \frac{v_o}{r_{o1}} = 0 \tag{2}$$

From (1) substituting for vgs in (2) and rearranging,

$$\frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}}}$$

$$= \frac{g_m r_{o1}}{1 + (g_m + g_{mb}) r_{o1} + \frac{r_{o1}}{r_{o2}}} \tag{3}$$

If load current source is ideal $r_{02} \rightarrow \infty$, (3) simplifies to

$$\lim_{r_{o2}\to\infty} \frac{v_o}{v_i} = \frac{g_m r_{o1}}{1 + (g_m + g_{mb}) r_{o1}} \tag{4}$$

If r_{o1} is finite, the open circuit voltage gain of source follower is less than unity even if body effect is neglected. The variation in output voltage changes the drain-source voltage and the current through r_{o1}. The large signal analysis shows that the over drive on gate also depends on the drain source voltage unless channel length modulation is negligible. This causes the small signal gain to be less than unity.

If $r_{o2} \rightarrow \infty$ and $r_{o1} \rightarrow \infty$,

$$\lim_{\substack{r_{o2}\to\infty \\ r_{o1}\to\infty}} \frac{v_o}{v_i} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\chi} \tag{5}$$

The (5) shows that the voltage gain of the source follower is less than unity and it depends on $\chi = g_{mb}/g_m$, which is in the range of 0.1 to 0.3. In addition, χ depends on source-body voltage, which is V_o when the body is grounded. Hence, gain found out in (5) depends on output voltage, causing distortion for large signal changes in the output. This can be overcome by selecting the type of source follower n-channel or p-channel fabricated in an isolated well. The well can be connected to source making $v_{sb} = 0$. In this case the parasitic capacitance from well to substrate increases reducing the bandwidth of source follower.

The output resistance of source follower can be calculated from Fig. 2 by driving the output with a voltage source v_o and setting $v_i = 0$.

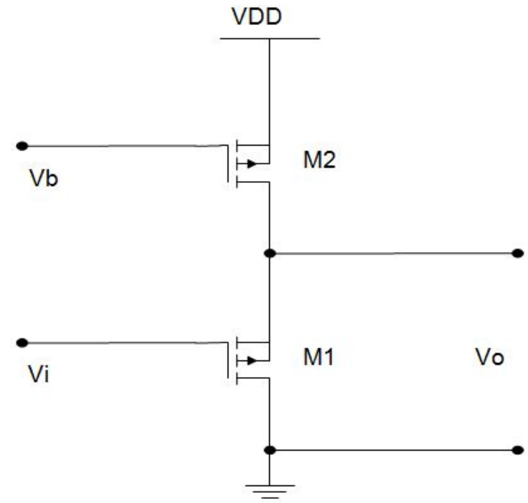

Figure 3. PMOS Source follower (PSF) circuit

$$i_o = \frac{v_o}{r_{o1}} + \frac{v_o}{r_{o2}} + g_m v_o + g_{mb} v_o v_0 \tag{6}$$

Then

$$R_o = \frac{v_o}{i_o} = \frac{1}{g_m + g_{mb} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \tag{7}$$

It is seen that the body effect reduces the output resistance, which is desirable as the source follower produces a voltage output. This desired effect results from the non-zero small signal current drawn by the g_{mb} generator. As $r_{02} \rightarrow \infty$, and $r_{01} \rightarrow \infty$, this output resistance becomes $1/(g_m + g_{mb})$, same as input resistance of common gate amplifier. The source followers are used as buffers and level shifters. They are more flexible as a level shifter because the dc value of V_{GS} can be change by aspect ratio W/L.

B. *Small signal analysis of PSF*

With the circuit of PSF, the most of designs have utilized a body tied PMOS input transistor to remove the bulk modulation effect and to improve the precision. This is possible as PMOS and NMOS transistors share the same substrate. Due to lower mobility of PMOS devices, this results in higher output impedance than NSF. Also the transconductance efficiency is low in PSFs which results into small drive ability and a larger silicon area.

Fig. 3 shows a conventional PSF in an n-well process which includes a PMOS input transistor and a PMOS current source. The small signal equivalent model for PSF will be same as NSF. In high frequency equivalent model, PSF will have additional capacitance due to bulk-well. In addition, the channel length modulation coefficients of M_1 and M_2 in PSF are smaller than that of NSF. This gives better linearity of PSF.

C. *The Super source follower*

The output resistance of source follower is approximately $1/(g_m + g_{mb})$ [3]. As MOSFETs have much lower transconductance, this output resistance may be too high especially when a resistive load is to be driven. The output resistance can be reduced by increasing aspect ratio W/L of

DOI: 01.IJCSI.4.2.1281

source follower and its dc bias current.

This requires a proportionate increasing the area and power dissipation. To minimize the area and power dissipation required for low R_o, the source follower configuration is used as shown in Fig. 3.

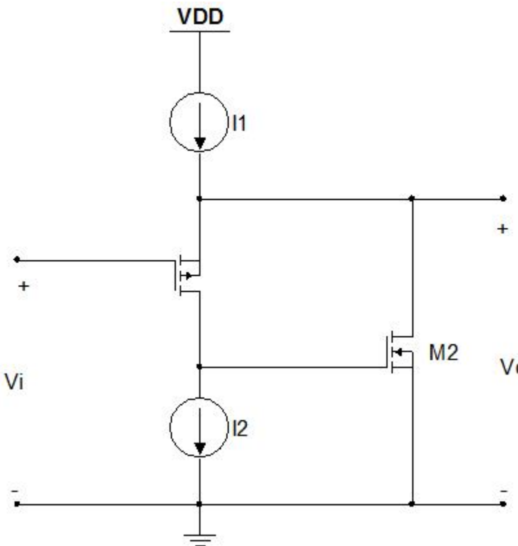

Figure 4. Super-source follower circuit

The super follower as shown in Fig. 4 uses negative feedback through M_2 to reduce the output resistance [4]. The qualitative analysis shows that, when the input voltage is constant and the output voltage increases; the drain current of M_1 also increases, resulting into increased gate-source voltage of M_2.

As a result, the drain current of M_2 increases, reducing the output resistance. The dc bias current in M_2 is the different between I_1 and I_2, therefore $I_1 > I_2$ is required for proper operation. This condition can be used to find small signal parameters of MOSFETs. The small signal equivalent circuit is shown in Fig. 5. The body effect of M_2 is neglected because $v_{bs2}= 0$. The polarities voltage controlled current sources for NMOS and PMOS are identical. The current sources I_1 and I_2 are replaced by their internal resistances r_1 and r_2 respectively. If current I_1 and I_2 are ideal, $r_{01}\rightarrow\infty$, and $r_{02}\rightarrow\infty$,. For practical current sources these resistances are large but finite.

To find output resistance of the super source follower, set v_i =0 and find the current i_o that flows into the output node when it is driven by a voltage v_o. Applying KCL at output under these conditions to Fig. 5,

$$i_o = \frac{v_o}{r_1} + \frac{v_o}{r_{o2}} + g_{m2} v_2 + \frac{v_2}{r_2} \qquad (8)$$

Similarly applying KCL at drain of M_1 with $v_i = 0$,

$$\frac{v_2}{r_2} - g_{m1} v_0 - g_{mb1} v_0 + \frac{v_2 - v_o}{r_{o1}} = 0 \qquad (9)$$

Substituting for v_2 from (9) into (8) and rearranging gives,

$$R_o = \frac{v_o}{i_o} = r1 \left\| r_{o2} \right\| \left(\frac{r_{o1}+r2}{[1+(g_{m1}+g_{mb1})r_{o1}](1+g_{m2}r2)} \right) \qquad (10)$$

Assuming I_1 and I_2 to be ideal current sources, also $r_{02}\rightarrow\infty$, and $(g_{m1}+g_{mb1})r_{o1}>>1$,

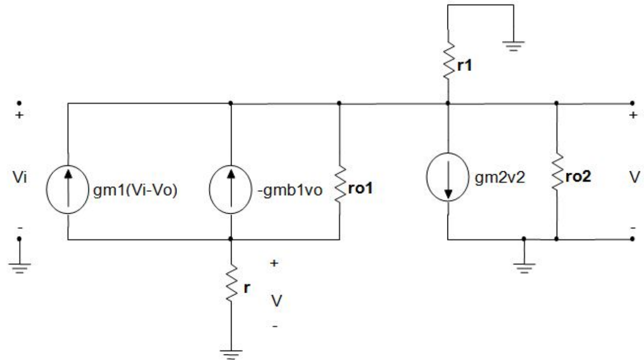

Figure 5.Small signal equivalent circuit of super source follower

$$R_o \simeq \frac{1}{g_{m1}+g_{mb1}} \left(\frac{1}{g_{m2} r_{o1}} \right) \qquad (11)$$

This is the output resistance of super source follower. Comparing (11) with the output resistance of source follower (7), shows that the negative feedback through M_2 reduces the output resistance by a factor of about $g_{m2}r_{o1}$.

The open circuit gain of super source follower can be found out from small signal equivalent circuit with the output open circuited. Applying KCL at the output node gives,

$$\frac{v_o}{r_1} + \frac{v_o}{r_{o2}} + g_{m2} v_2 + \frac{v_2}{r_2} = 0 \qquad (12)$$

Also applying KCL at drain of M_1 gives

$$\frac{v_2}{r_2} + g_{m1}(v_i - v_0) - g_{mb1} v_0 + \frac{v_2 - v_o}{r_{o1}} = 0 \qquad (13)$$

Substituting for v_2 from (12) into (13) and rearranging gives

$$\frac{v_o}{v_i} = \frac{g_{m1} r_{o1}}{1+(g_{m1}+g_{mb1})r_{o1} + \frac{(r_2+r_{o1})}{(r_1 \| r_{o2})(1+g_{m2} r_2)}} \qquad (14)$$

With ideal current sources,

$$\frac{v_o}{v_i} = \frac{g_{m1} r_{o1}}{1+(g_{m1}+g_{mb1})r_{o1} + \frac{1}{g_{m2} r_{o2}}} \qquad (15)$$

Comparing the open circuit voltage gain of the super source follower (15) with the open circuit voltage gain of a simple source follower (4) shows that the deviation of this gain from unity is greater in super source follower than a simple source follower. If $g_{m2}r_{o2}$ >>1, this difference is small and the conclusion is that the super source follower has little effect on the open circuit voltage gain. The product $g_m r_o$ for MOSFET is given by relation

$$g_m r_o = \sqrt{2\mu C_{ox} \left(\frac{W}{L}\right) I_d / (\lambda I_d)} \qquad (16)$$

Where μ is mobility of charge carriers, Cox is gate oxide capacitance, λ is channel length modulation coefficient and W/L is aspect ratio

In addition, λ α 1/L, hence we get

$$g_m r_o \propto \sqrt{\frac{WL}{I_d}} \qquad (17)$$

Therefore the width and length can be adjusted to get desired product $g_m r_o$ without changing I_d.

III. Proposed circuits

A. NSF with current source load

The circuit of NSF is formed with load resistance replaced by simple MOS current source using M_2 as shown in Fig. 6. This current source offers high resistance if operated in saturation region [6]. The voltage applied at gate of M_2 that is V_b makes sure that M_2 operates in saturation all the time [10]. The source follower circuit is designed with dc bias drain current of 1mA and dc level shift of 0.43V with supply voltage 2.5V. Then using basic equation for drain current, aspect ratio of M_1 and M_2 is calculated as 200/0.45 (μm/μm) for M_1 and 60/0.45 (μm/μm) for M_2 and applying dc voltage V_b = 0.6V.

The circuit is simulated using EDA tool Tanner V14.1 with 0.25 μm technology and Cadence with 0.18 μm technology. The small signal voltage gain as per simulation of the circuit comes out to be 0.8323 and output resistance comes out to be 9.1k&!. In addition, bandwidth is measured which comes out to be 350MHz.

The result shows large deviation of small signal voltage gain from unity and the higher output resistance as compared to emitter follower

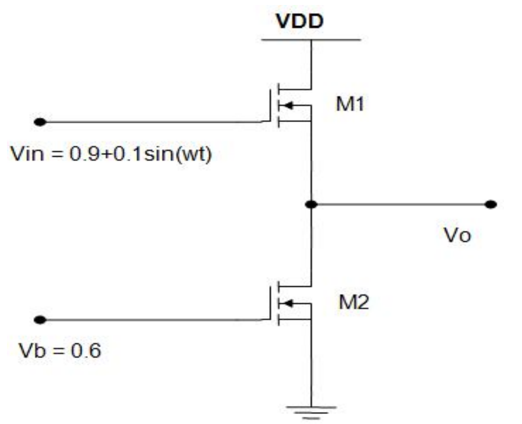

Figure 6. NSF with current source load

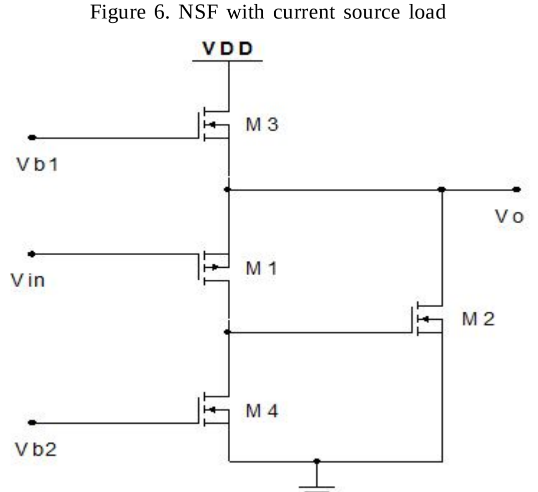

Figure 7. Super source follower with current mirror sources

B. PSF with current source load

The circuit of PSF is formed with load resistance replaced by simple MOS current source using M_2 similar to NSF. The PSF circuit is designed with dc bias drain current of 1mA and dc level shift of 0.8V with supply voltage 2.5V. Then using basic equation for drain current, aspect ratio of M_1 and M_2 is calculated as 500/0.49(μm/μm) for M_1 and 60/0.49 (μm/μm) for M_2, moreover, applying dc voltage V_b = 0.6V.

C. SSF with current source load

For super source follower M_1 is selected with aspect ratio 500/0.5 (μm/μm), being PMOS with bias current 1mA. Both current sources I_1 and I_2 (Fig. 4) are implemented using single MOSFETs M_{-3} and M_4 as shown in Fig. 7. The total current supplied by upper current source M_3 is addition of dc bias current required for M_1 and dc bias current required for M_2. As M_2 provides negative feedback for super source follower circuit, it is desired to draw less amount of current. Hence the dimensions of M_2 is selected 1/1 (μm/μm). This selected W and L of M_2 will ensure small feedback current through M_2 with high $g_m r_o$ as per (16) and (17). The dc bias current of M_1 is 1mA, thus the dimension of M_4 is selected W/L=60/0.5 (μm/μm) with gate bias V_{b2}= 0.6V. The aspect ratio of M_3 is selected to be 120/0.5 (μm/μm) with gate bias V_{b1}=1.9V to supply desired bias currents to M_1 and M_2. The result of simulation gives a small signal voltage gain 0.42 and the output resistance 4.7k&! which is lower than that of NSF and PSF. The bandwidth measured shows 800MHz, larger than that of NSF and PSF as expected. The dimensions of MOSFETs selected for three circuits are shown in Table I and simulated results are shown in Table II.

Table I. Dimensions of mosfet devices

MOSFETs	Aspect Ratio (W/L) μm/μm		
	NSF	PSF	SSF
M_1	200/0.45	500/0.49	500/0.5
M_2	60/0.45	60/0.49	1/1
M_3	----	----	120/0.5
M_4	----	----	60/0.5

Table II.simulated results

Parameters	Simulated results		
	NSF	PSF	SSF
Voltage gain A_v	0.8323	0.909	0.42
R_{out}	9.1kΩ	9.9 k Ω	4.7k Ω
Bandwidth	350 MHz	200 MHz	800 MHz

IV. Conclusions

It is observed from simulated results that voltage gain of PSF comes out to be closer to unity than NSF. While the bandwidth offered gets reduced in PSF. The other important performance parameter, the output resistance is measured lowest with SSF but at the cost of reduced voltage gain.. The voltage gain of super source follower gets reduced by almost same proportion as that of output resistance. The super source follower is useful in driving low input resistance loads. It is also used in bipolar technologies to reduce the

current conducted in a weak pnp transistor load. Due to use of long channel device M_2 at output, the higher junction capacitances may shunt the output reducing bandwidth of the circuit. The proposed circuit can be used as a level shifter output stage in operational/instrumentation amplifiers with lowered output resistance. The circuit is operated with supply voltage V_{DD}=2.5V.

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DOI: 01.IJCSI.4.2.1281